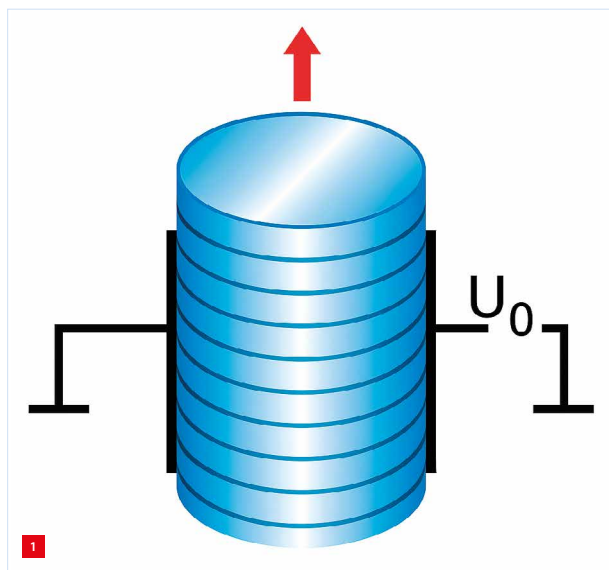


ADVANCEMENT POWERED BY PIEZO

Current semiconductor equipment and future innovations require precise and reliable equipment to address the continuing push for miniaturised chips and increasing chip demand. This article dives into the pivotal role piezoelectric systems play in solving the challenges of cost reduction and process improvement so that the semiconductor industry can continue to be at the forefront of innovation and advancements in new technologies.



A piezoelectric stack actuator made of stacked ceramic discs is shown. Electrodes are attached to either side and a voltage U_0 is applied. The direction of motion in the axial direction is highlighted in red. (Source: [1])

Introduction

The semiconductor manufacturing industry stands at the forefront of innovation, allowing advancements in information processing, communication, and emerging technologies such as artificial intelligence and electric vehicles. This advancement in current and emerging technologies requires a manufacturing focus on maintaining and increasing precision to develop smaller, faster and more efficient chips. Each step of the semiconductor manufacturing process has unique challenges and production steps that require innovative solutions. One challenge is evident across all manufacturing steps: the impact due to the demand for smaller, denser and faster chips.

Moore's law states that the transistor count on an integrated circuit doubles every two years. This law has held up until recently, as transistor sizes have approached the size of a few atoms wide, challenging the laws of molecular physics. The main concern is quantum tunnelling, which disrupts the insulating/conducting properties of neighbouring atoms within the transistors.

Nonetheless, there still is an industry-wide focus on miniaturisation that encourages cost reduction and process improvements, which define the semiconductor industry. This article dives into the pivotal role piezoelectric systems play in solving these challenges.

Piezo basics

A clear grasp of piezo theory is needed to understand the utilisation of piezoelectric technology within semiconductor manufacturing. The piezoelectric effect occurs when certain crystalline materials produce an electric charge when subjected to mechanical stress. Conversely, the inverse piezoelectric effect occurs when a material deforms due to an applied electric field.

Piezoelectric actuators utilise the inverse piezoelectric effect in the application of piezo stacks made of stacked ceramic discs that are laminated and connected in parallel. When utilising materials such as PZT (lead-zirconate-titanium), these piezo stacks will expand in the axial direction of the stack with an applied electric field (Figure 1). The current applied to the stack deformation predominantly determines the speed of the piezo-stack operation. Piezo stack design allows customisation such as incorporating a central hole to encourage airflow or if access is needed. These piezo stacks can be constructed as bare stacks, encased stacks with a mechanical preload, or integrated into other designs such as multi-axis stages with the addition of flexure hinges to translate high-motion profiles. Examples of various piezoelectric products are shown in Figure 2.

Advantages and disadvantages

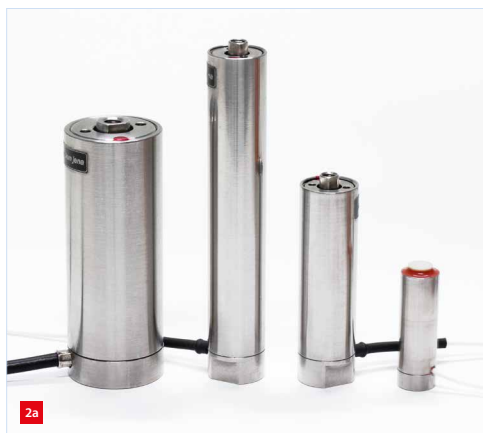
Piezo advantages include:

- low sub-nanometer precision;
- high compressive strength;
- lifetime durability;
- low maintenance;
- high force outputs with high actuation speeds.

EDITORIAL NOTE

This article was contributed by piezosystem jena, located in Jena (Germany), which is represented by Te Lintelo Systems in the Netherlands.

www.piezosystem.com
www.tlsbv.nl



Examples of various piezoelectric products. (Source: [2])
 (a) Collection of stacks with varying degrees of width and length.
 (b) Objective positioner used for objective autofocusing.
 (c) Stage positioner used for wafer-chuck handling.

Piezo disadvantages include:

- hysteresis and creep;
- risk of depolarisation;
- low tensile and torque strength;
- expensive cost.

Solutions to these problems include:

- closed-loop measurement systems;
- active cooling;
- preloads to withstand torque/tensile forces.

Applications

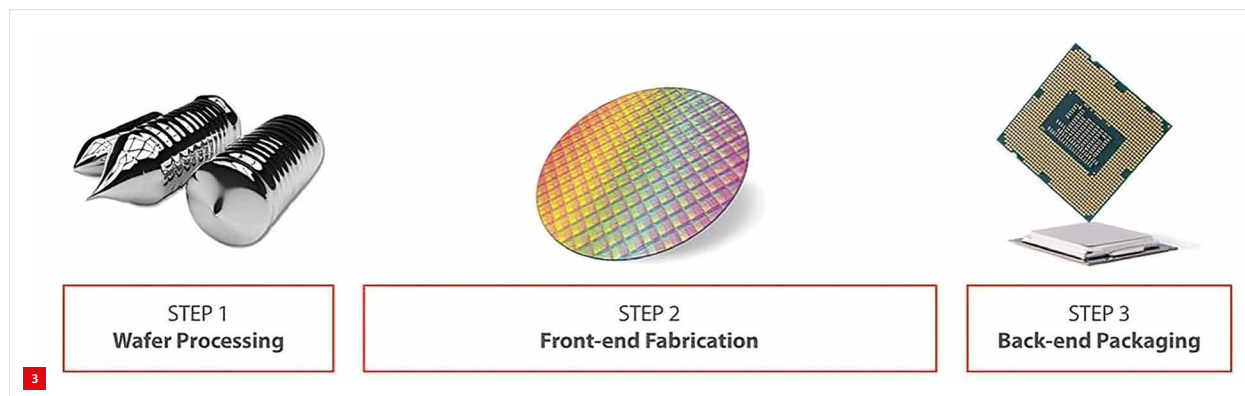
Front-end processes

Figure 3 gives an overview of the large steps in the semiconductor manufacturing process. Piezo objective positioners can be used to inspect wafer thickness during wafer-slicing processes. The thickness range is typically between 280 and 725 micrometers [3]. Piezos are capable of enabling precise inspection of the entire thickness with nanometer accuracy when integrated with a closed-loop feedback control. Also, wafer polishing is possible with high-powered piezo stacks by integrating a polishing head to drive the actuator at high frequencies, in the kHz range.

These stacks enhance wafer smoothness while minimising defect densities and reducing wafer warpages.

A new application of piezo technology is used during the deposition phase of die fabrication, specifically chemical vapour deposition (CVD). As different photoresist layers are deposited onto the silicon wafer, chemical vaporisers are used to heat and effectively spray sub-micron-thick layers onto the silicon wafer. As photoresist processes become more advanced, the deposition process requires faster and thinner deposition layers. Therefore, the chemicals sprayed onto the wafer need to be finely vaporised requiring fast, precise and consistent delivery systems. One way to increase precision is by using compact stack actuators as the valve device within the chemical plumbing. These actuators are used for fast actuation and can be operated for hours at a time without wear or misalignment.

The applications with the highest potential for piezoelectric system implementation are inspection in general and defect inspection in particular. For inspection use, objective positioners will autofocus the desired target to ensure proper alignment and placement while locating potential



Overview of the semiconductor manufacturing process. Silicon ingots are processed into wafers during step 1, dies are fabricated during the front-end of the process, and finally dies are packed into packaged devices during back-end packaging. (Source: [4])

defects. Objective positioners extend microscopy inspection by ensuring a sub-nanometer resolution with a total travel range of several hundreds of microns and loads up to several hundreds of grams. Additionally, high-load-capacity stages offer nanometer-level resolution to adjust the wafer-chuck positioning.

There are three main inspection areas where piezo systems offer improvements:

1. Mask inspection:

The mask contains intricate circuit patterns that require a high-quality and flawless stencil made of glass or fused silica with an opaque film that needs to be projected onto wafers precisely [5].

2. Defect inspection:

Once the mask projects the pattern to the wafer, the pattern needs to be free from defects or inconsistencies. High resolution and fast dynamics are needed to ensure defects are detected early in the process before multiple layers are projected to prevent major disruptions in downstream performance. The defects could include discrepancies between the expected pattern and the observed pattern on the wafer post-mask inspection. These defects are not solely due to circuit-design defects, but also to discrepancies created due to the transfer of the mask onto the wafer.

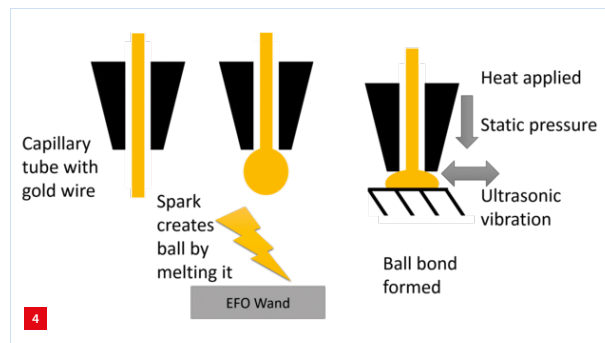
3. E-beam inspection:

With the development of smaller chip architectures, lithography patterns become smaller and harder to inspect. E-beam machines utilise electron beams to project onto the smallest features of the die that optical inspection tools cannot detect. These sensitivities are often smaller than 1 nm and can be supplemented with piezo-wafer positioners to align the electron beam to the dies. Objective positioners can be implemented to adjust objectives used in the E-beam apparatus. Often, this application is used in R&D machines separate from in-line manufacturing processes to solve current problems on the manufacturing line.

All these tools increase precision, reduce defect-analysis time, and improve process output. Overall, die fabrication is a lengthy step in the semiconductor manufacturing process that includes many interconnected processes, such as lithography, inspection and defect analysis. These systems combat many of the processes challenged with a miniaturised and efficient solution via stack actuators or objective positioners.

Back-end processes

Once semiconductor wafers have been processed and the dies have been cut in a process called dicing, the dies move to the packaging step of the manufacturing process. This is the final step to transform delicate silicon chips into robust



A simplified wire-bonding process in three steps. First, a gold wire is placed in a capillary tube. Then, a spark is created by an EFO (electric flame off) wand that melts the gold wire into a sphere. Finally, with applied heat and sonic pressure, an ultrasonic vibration is introduced to form a bond between the spherical gold ball and the substrate.

components for real-world applications. Aside from potential positioning applications in this phase, piezo-electric systems can be utilised effectively in two main areas: fine-pitch bonding during packaging, and device cleaning for removing contaminants caused by advanced packaging structures.

Wire bonding (Figure 4) is a critical step during packaging that connects individual dies to external circuitry, linking the micro-scale of the semiconductor devices to the macro-scale of electronic devices. After dicing, individual dies are attached to a lead frame that serves as the device's structural and electrical interface. Since this is a delicate process analogous to microscopic soldering, fine bonding must occur without any additional materials added that would otherwise render the circuit compromised.

Ultrasonic energy must be used to create a metallurgical bond that is durable and miniature. Piezoelectric actuators can generate ultrasonic frequencies to facilitate this process ensuring precision, repeatability and reliability. Once bonded, various protective moulds are added to avoid environmental damage. These actuators are miniature and can produce high-repeatability ultrasonic signals with highly tuneable frequency responses to encourage varying degrees of wire bonding.

One example during the production of advanced memory structures includes the challenge of cleaning confined hidden surfaces. Companies have developed bubble oscillation technologies to address these challenges by introducing controlled bubbles to clean hard-to-reach areas through the precise control of bubble cavitation. Features are not damaged during cavitation, which reduces failure rates and increases cleaning throughput.

High-powered piezoelectric actuators and shakers are a potential solution to increase the success of bubble-cavitation technologies [6]. Because of precise actuator

signal outputs, compact device size, and lifecycle, piezoelectric shakers are a potential solution for these technologies. While these processes tend to use a megasonic frequency range (20-80 kHz), piezoelectric actuators and shakers are capable of reaching a more precisely defined frequency range, of about 70 kHz or even 100 kHz, with a smaller bandwidth. This improves the cavitation process productivity and efficiency to address device scaling, complex structures, and the integration of new materials.

There is a compelling case for integrating piezoelectric systems into post-wafer processing and device fabrication due to precision, reliability and versatility. As the industry grapples with new complexities of 3D structures, high aspect ratios, and other challenges, the precise frequency generation and reliability of piezoelectric technology may provide solutions to back-end packaging for the semiconductor manufacturing industry.

Challenges

Piezoelectric technology has made significant progress in advancing precision, durability and reliability in semiconductor manufacturing. Integrating this technology does not come without its challenges. Operational factors, integration and compatibility with existing equipment, and cost-benefit analysis all need to be considered to fully assess this technology's challenges.

While piezoelectric systems offer sub-nanometer precision, this technology does operate under certain environmental and mechanical constraints. First, ceramic materials must not be heated past their Curie temperature (150-350 °C), or their piezoelectric properties will be diminished. In high-temperature environments, this requires the use of forced air or non-water liquid for active cooling. In some cases where space is limited, this may introduce additional complexity and spatial requirements. Moreover, piezoelectric systems will need special adaptations to operate under vacuum or cleanroom conditions. Luckily, the ceramic will function fine in vacuum; cables/leads, however, will have to be replaced with materials that do not outgas and increase the ultra-low vacuum pressures.

The push towards smaller structure sizes results in higher technical requirements that are far beyond resolution improvements. Since semiconductor processes require precision imaging, all symmetry aspects of nanopositioning optics must be accurate. This includes straightness of motion, cross-axis motion, and lateral run-out. The entire motion profile of a piezo system must have improved linearity, so there is minimal drift of the desired set position. This will require measurement systems in closed-loop configurations that have the highest linearity properties,

which could induce additional costs. Proper installation is imperative as piezo electrodes may drift into the ceramic during dynamic conditions.

Conclusion

Piezoelectric technology has seen recent success in the semiconductor manufacturing industry, yet has not fully captured the full potential of implementation. Manufacturers of piezo systems operate at the limit of mechanical and material properties to develop the next level of high-precision positioning tools. Experts in materials science and mechanical systems should collaborate to push the limits of static and dynamic positioning applications. As piezoelectric technology evolves, it leads to further streamlined processes. With the intricate evolution of 3D chip designs, and multi-layer chip architectures, the precision of piezoelectric systems may become foundational. Their advancements and integration capabilities are not merely a trend, but a cornerstone of future development.

As the semiconductor industry advances into a new era founded on further chip miniaturisation, and increased focus on efficiency, piezoelectric systems are at the forefront of this advancement, bridging the gap between precision and reliability once thought unattainable into real-world applications. The capabilities of this technology provide precision at the sub-nanometer scale enhancing wafer preparation, chip imperfections, and advanced packaged solutions.

While the decline of Moore's Law may impact the industry in new ways rarely seen before, piezoelectric technologies emerge as a readily available and future-forward solution to address complex modern challenges at the intersection between materials science and mechanical engineering. Due to the complexity of semiconductor manufacturing, and application-specific technical requirements for piezo technology, further collaboration between semiconductor and piezo manufacturers is needed to ensure the semiconductor industry continues to innovate and push the boundaries of chip miniaturisation.

REFERENCES

- [1] www.piezosystem.com/piezopedia/design
- [2] www.piezosystem.com
- [3] Microchemicals, *Basics of Microstructuring*, retrieved 20 October 2023, www.microchemicals.com/dokumente/application_notes/silicon_wafer_production_specification.pdf
- [4] www.semiceramic.com/semiconductor-grade-ceramics-enable-future-electronics
- [5] Semiconductor Engineering, *Photomask*, retrieved 20 October 2023, www.semiengineering.com/knowledge_centers/manufacturing/lithography/photomask
- [6] David, H.W., and Lei, H., "Damage-Free Cleaning of Advanced Structure Using Timely Energized Bubble Oscillation Megasonic Technology", *Solid State Phenomena*, vol. 282, pp. 64-72, 2018, [www.doi.org/10.4028/www.scientific.net/SSP.282.64](https://doi.org/10.4028/www.scientific.net/SSP.282.64)